

What If the Biggest AI Payoff Is Not Inside the Chip?

Using AI Across Design, Testing, Knowledge Management, and Transition

RHET 2026 Workshop

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Artificial intelligence in advanced electronics is often discussed in terms of putting AI into the final product. But in radiation-hardened electronics, the larger near-term opportunity may be the engineering enterprise surrounding the chip: requirements, customer needs, design, simulation, fabrication, radiation testing, analysis, qualification, transition, and sustainment. This interactive workshop will examine how AI can connect these activities, reduce engineering bottlenecks, and shorten the design-test-redesign cycle.

Practical examples will include AI-assisted analog design, code and test-bench generation, secure engineering workflows, radiation-test analysis, interfacility correlation, adaptive testing, and preservation of engineering knowledge. A particular focus will be on AI as a persistent engineering memory—capturing requirements, design intent, raw test data, methodology, configuration, and the reasoning behind engineering decisions so that context is not lost between organizations or over time.

The workshop will also deliberately make AI fail by withholding critical information and allowing it to generate a convincing but incorrect conclusion. That demonstration will lead into a discussion of assurance, data security, physics constraints, human technical authority, and surety.